Prior Art: Parallel VID Communication

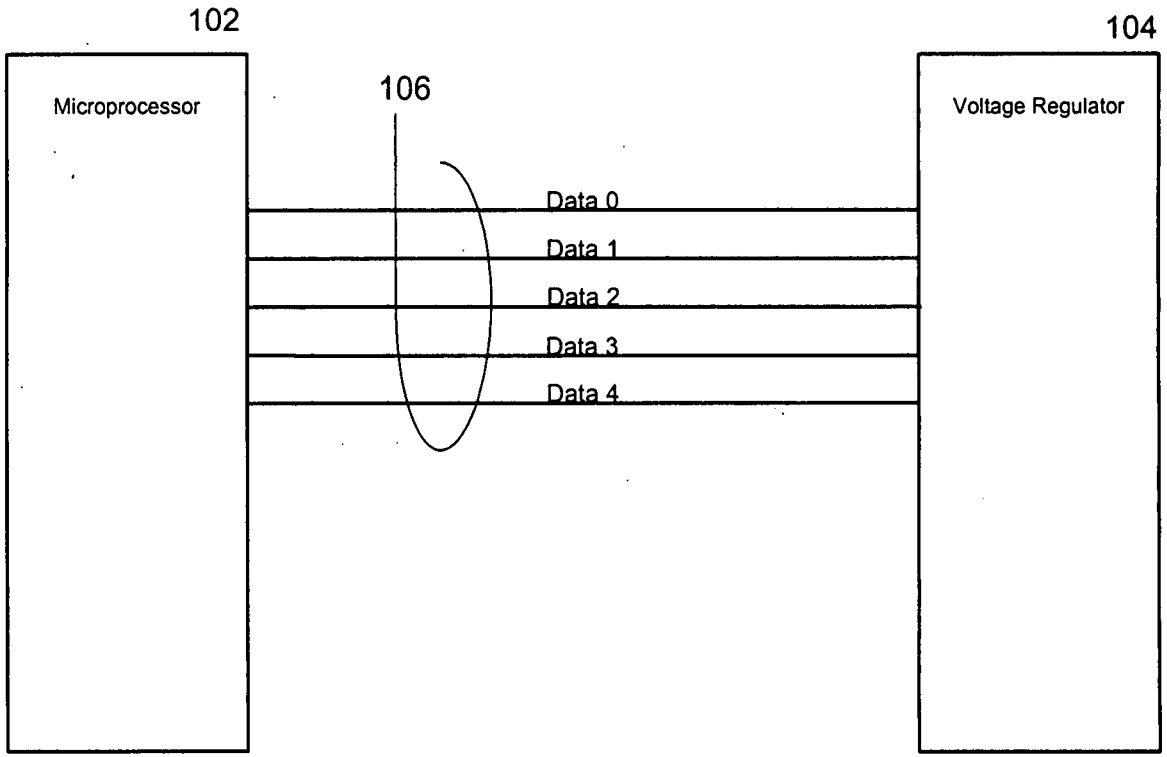

Figure 1

Fig 1 Formal Drawings
3/14/02

Prior Art: SM Bus

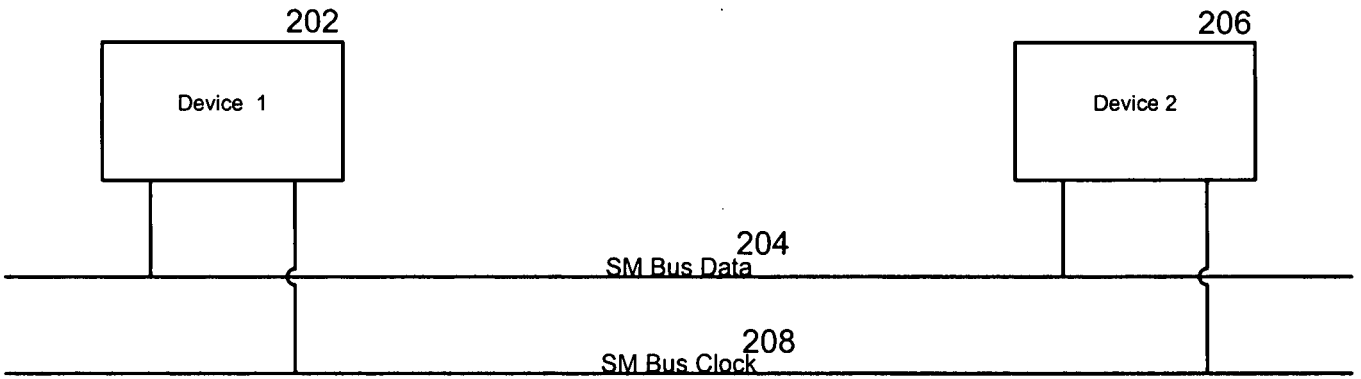

Figure 2

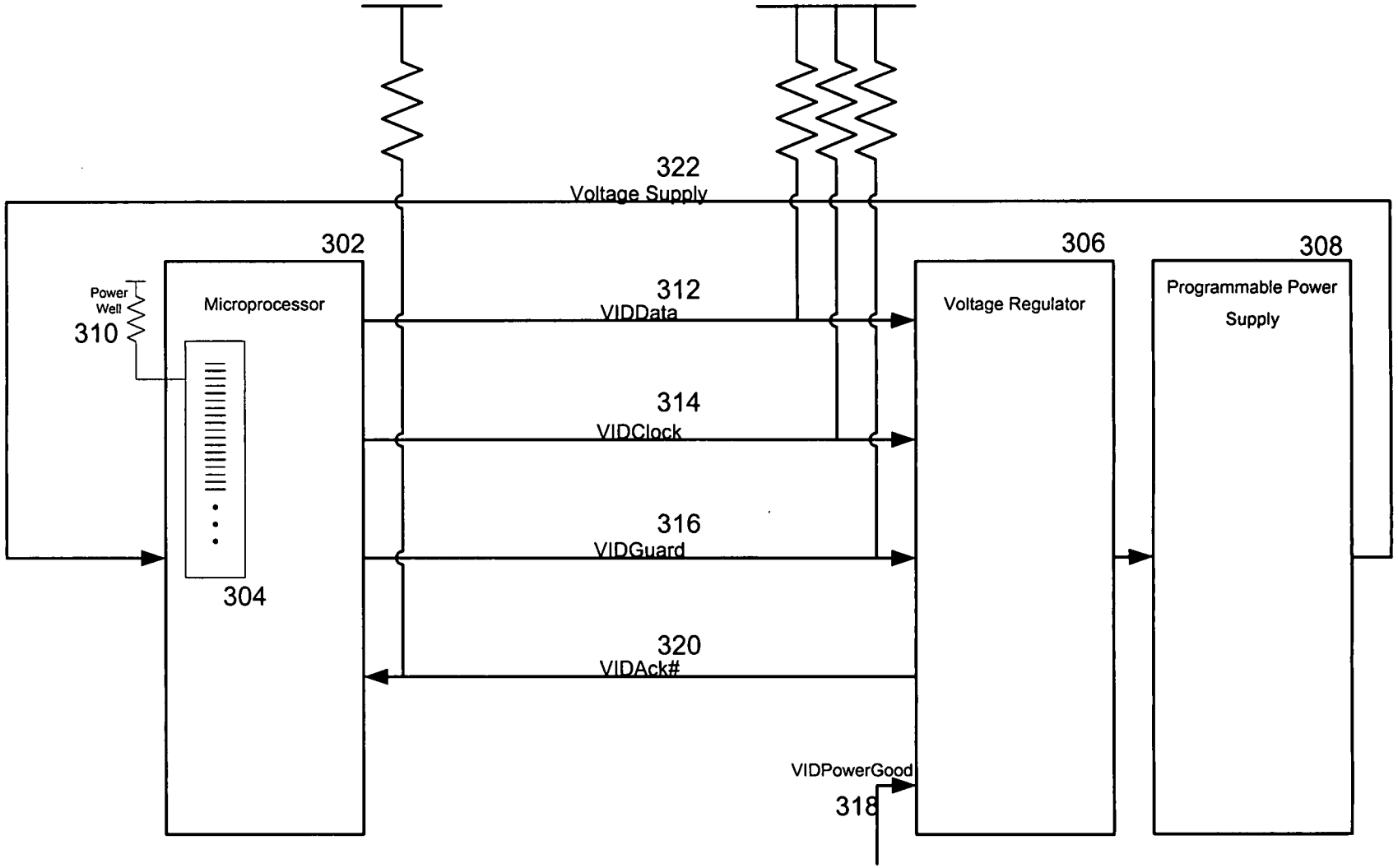
Serial VID Interface
322
Voltage Supply
302
Microprocessor
Power Well
310
304
312
VIDData
314
VIDClock
316
VIDGuard
320
VIDAck#
306
Voltage Regulator
308
Programmable Power Supply
VIDPowerGood
318

Figure 3

VIDData and VIDGuard Timing

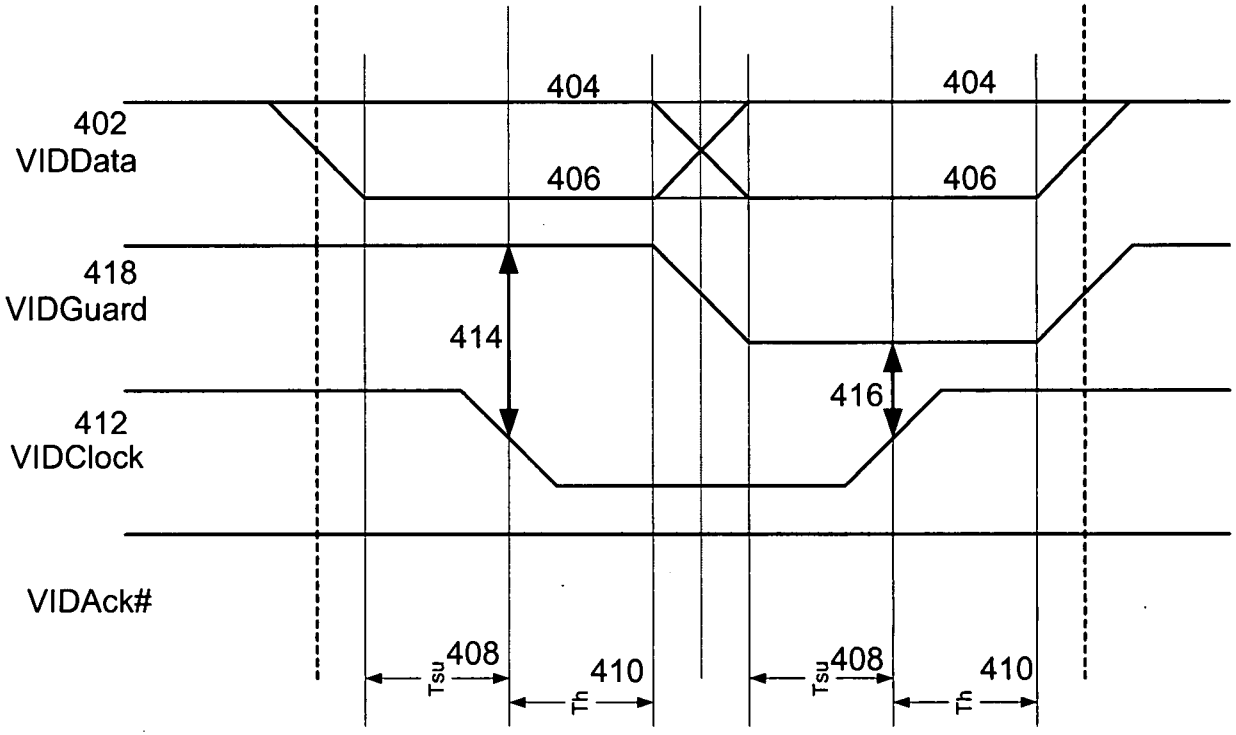

Figure 4

VIDAck# Timing

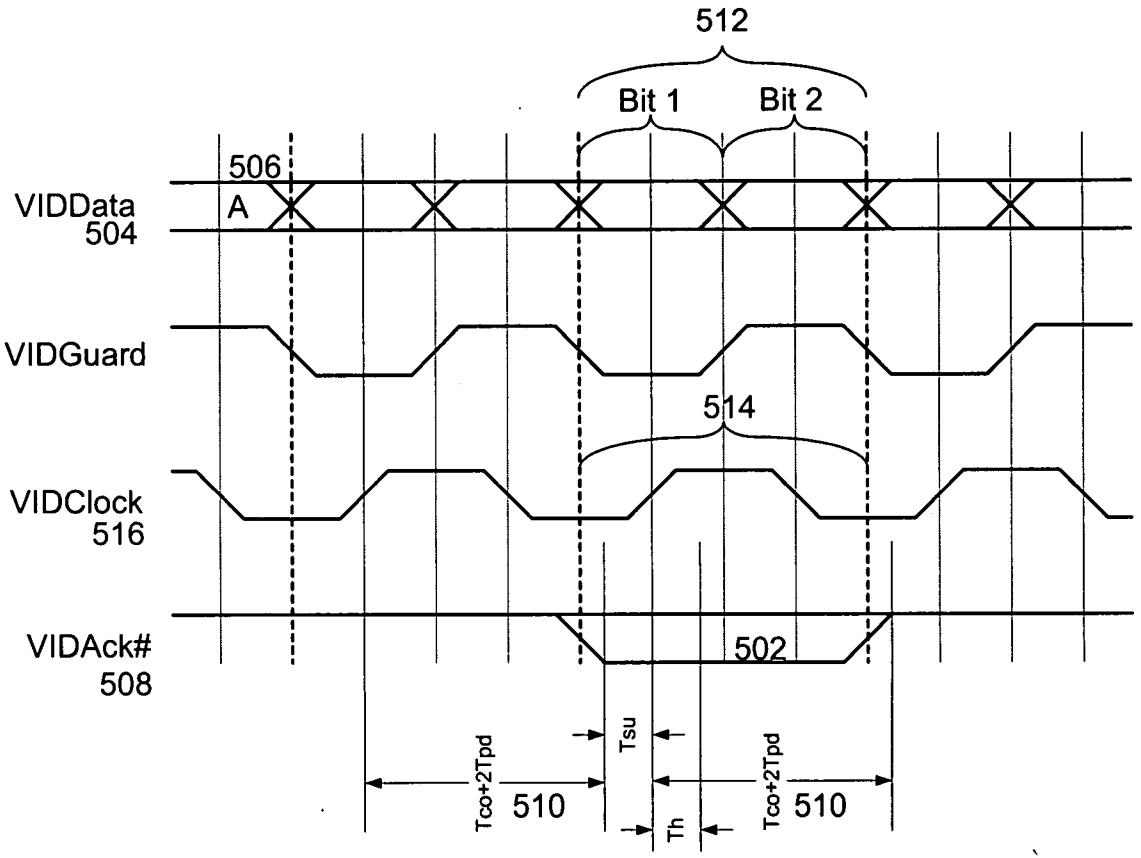

Figure 5

Prior Art: SM Bus

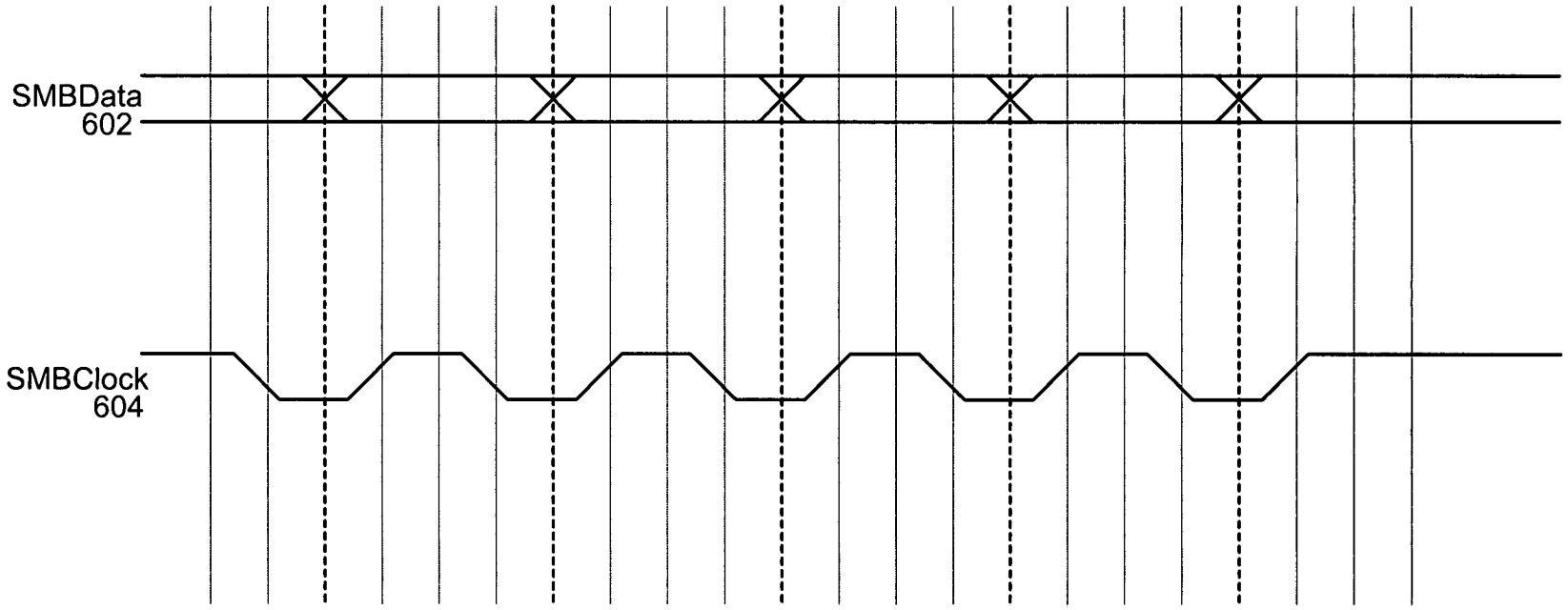

Figure 6

Command Byte

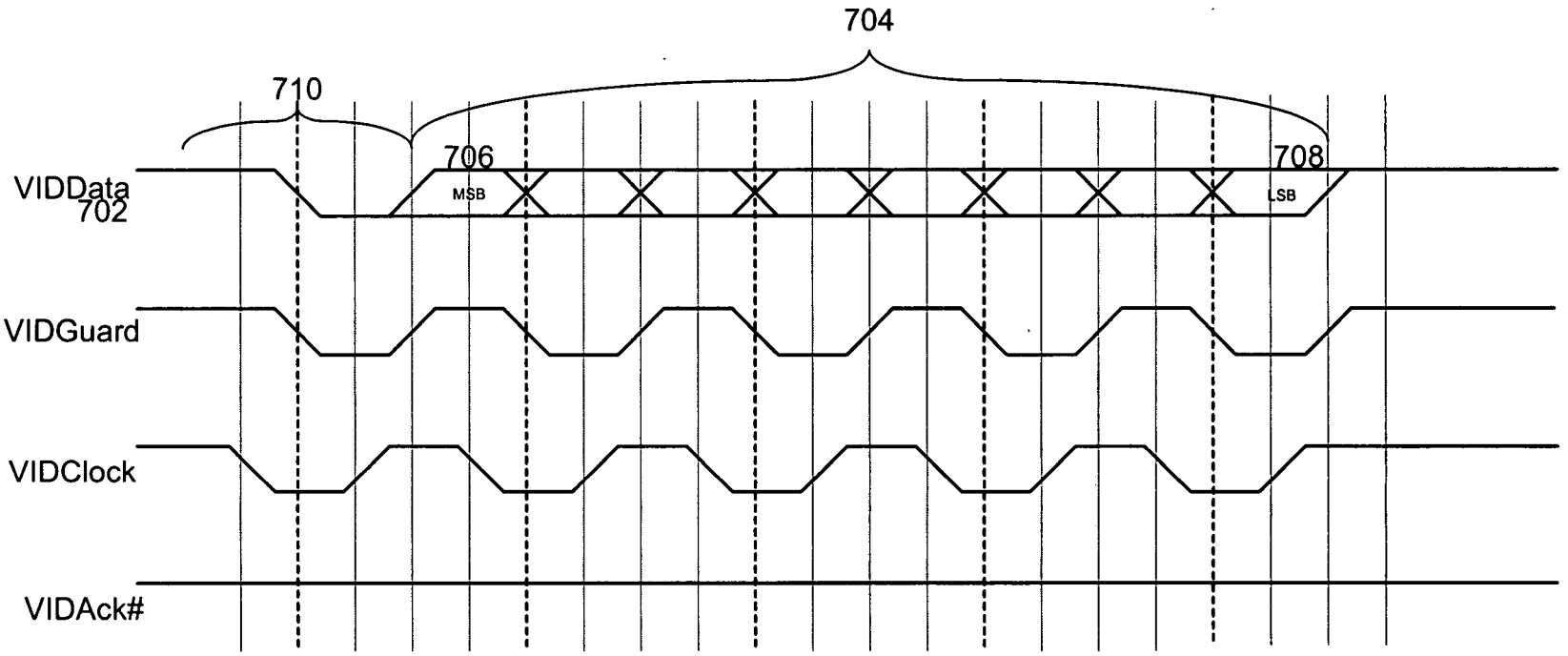

Figure 7

Data Out Byte

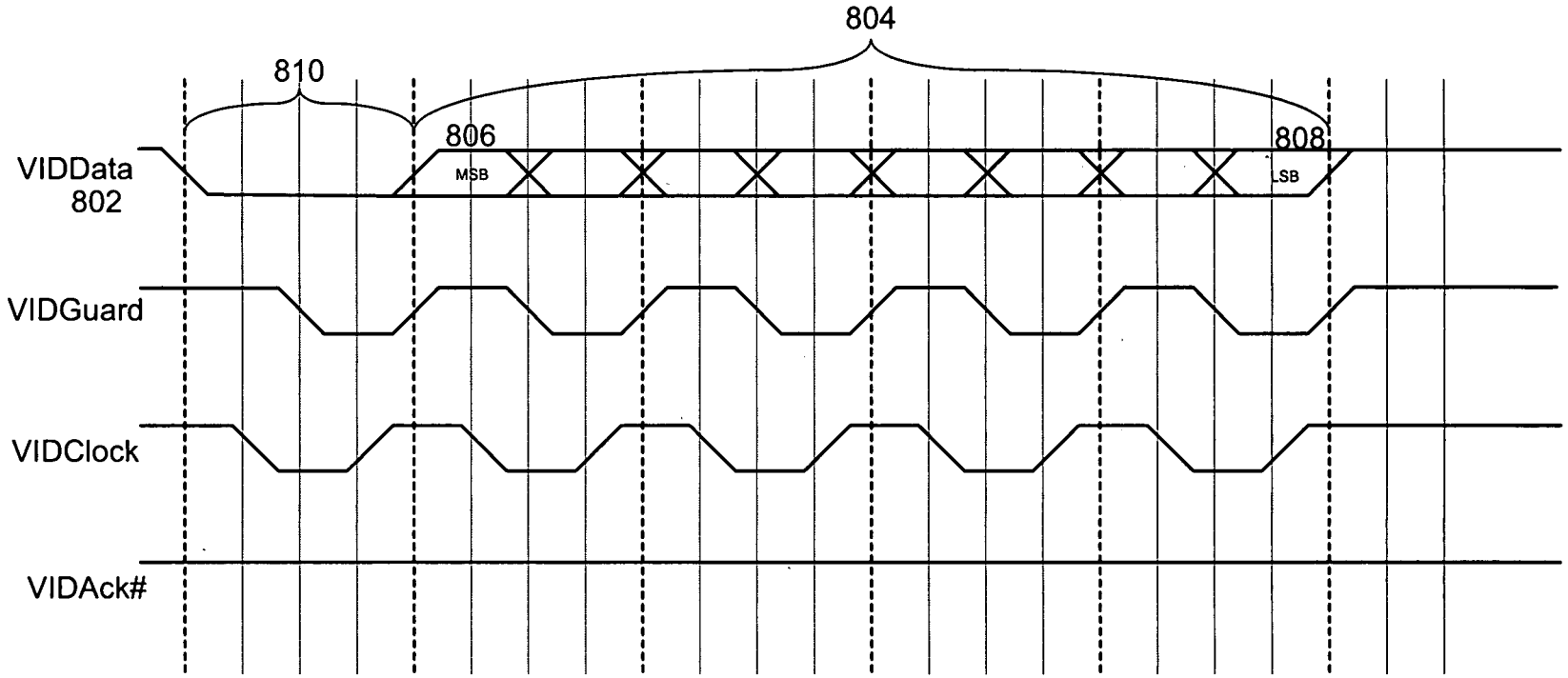

Figure 8

CRC-8 Byte

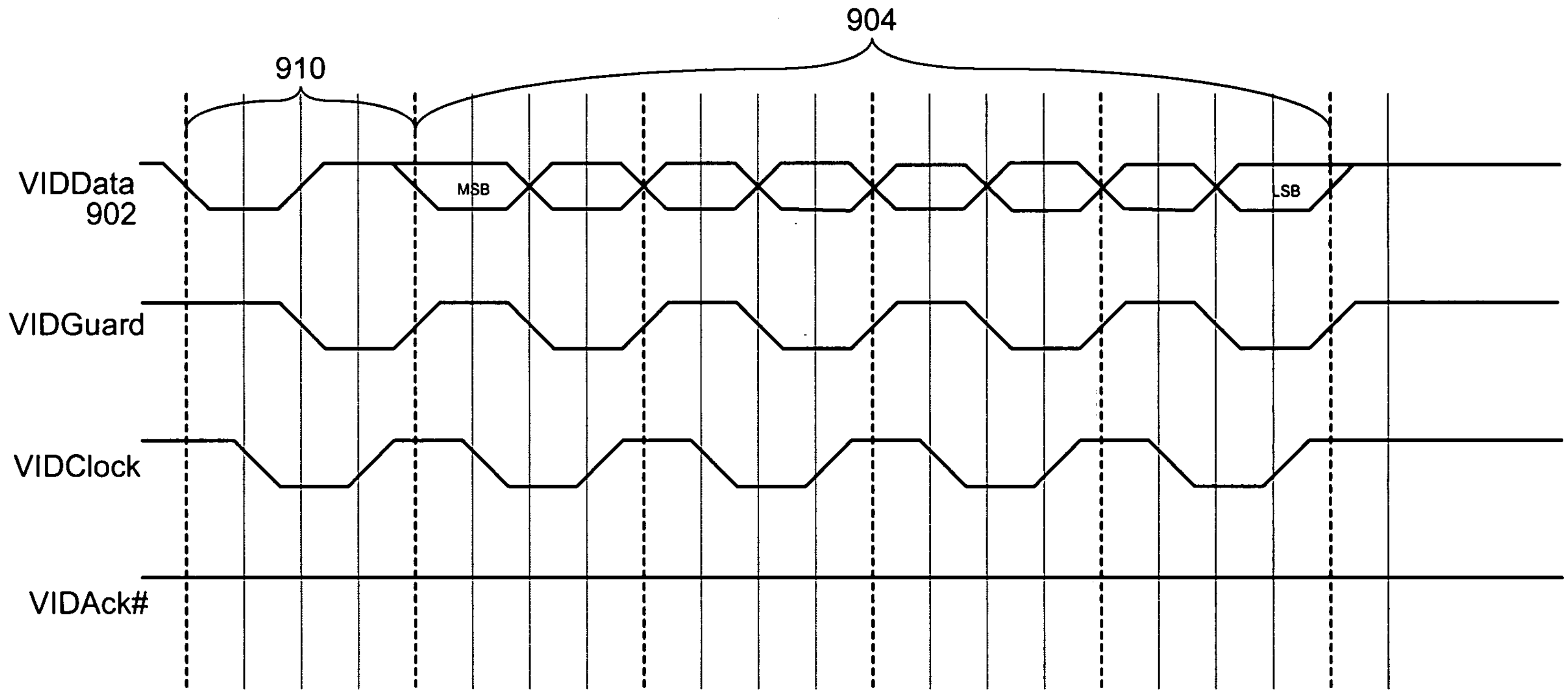

Figure 9

Ack Byte with Positive Acknowledgement

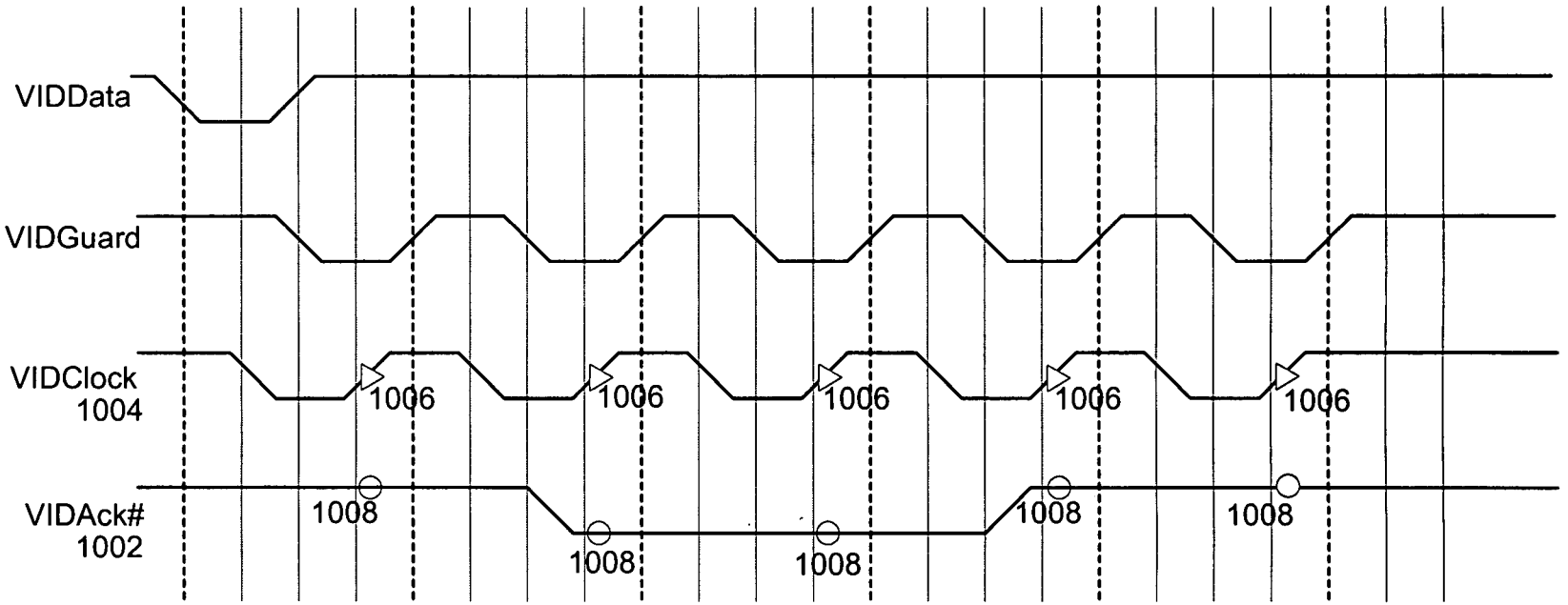

Figure 10

Sync Byte

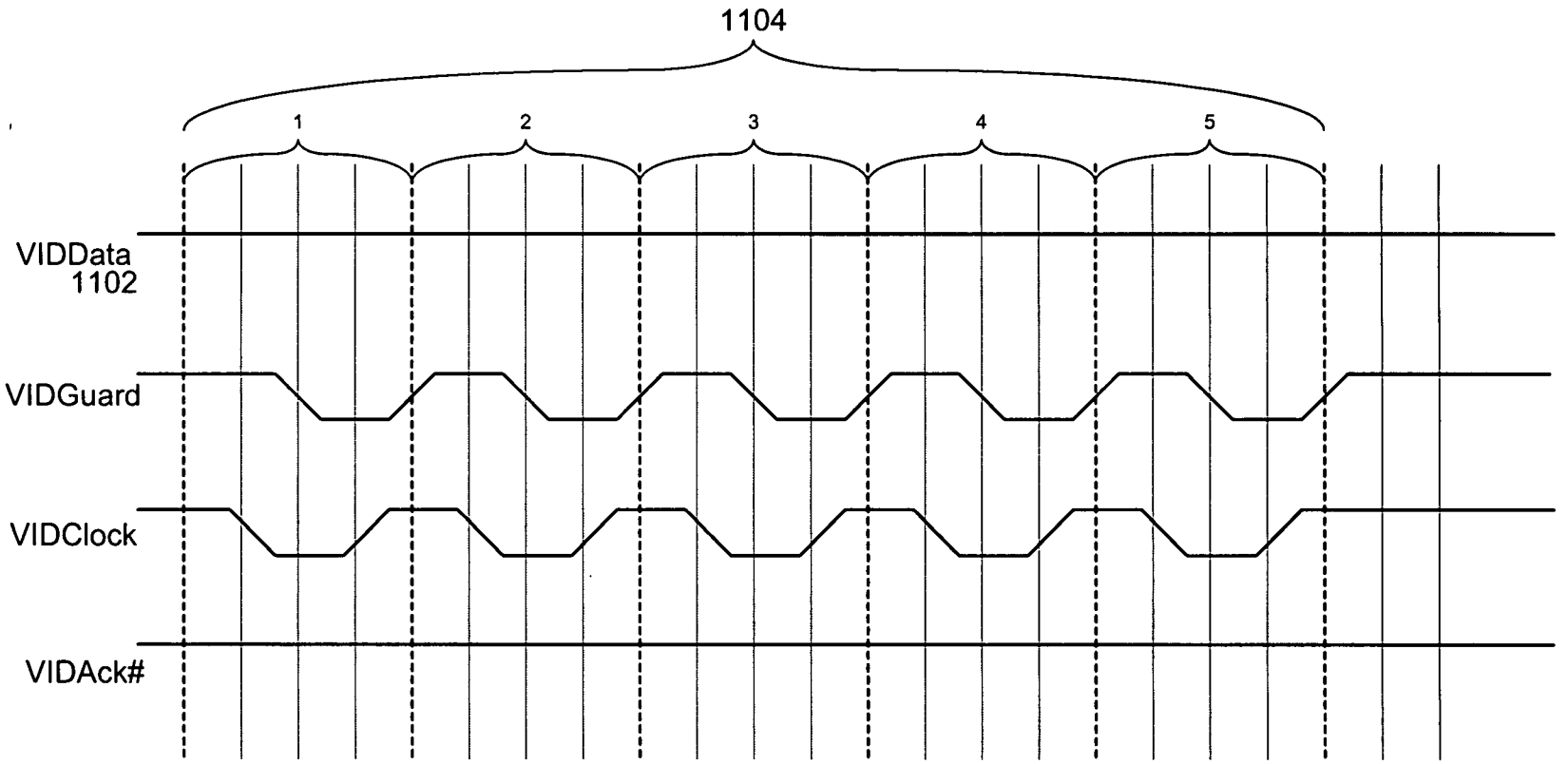

Figure 11

Complete Command

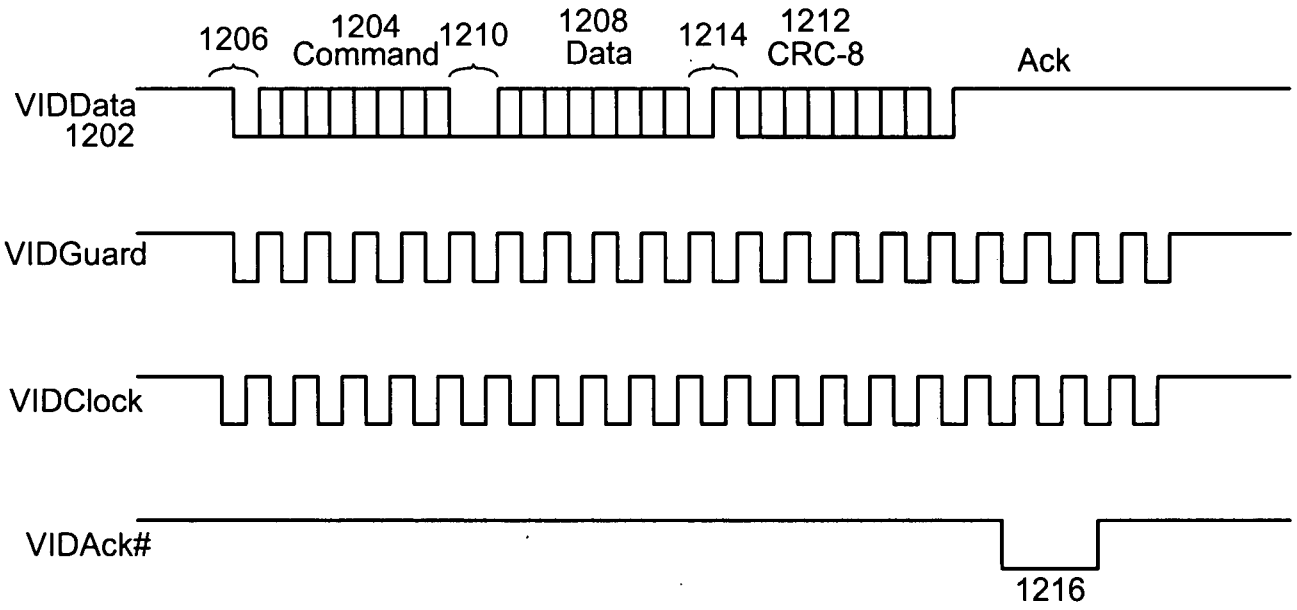

Figure 12